WHAT IS CLAIMED IS:

1. A method for functionally controlling the program and/or data flow in signal processors, wherein the signal processors have respective closed modules that are separate from one another, are intended for program and data flow control, and operate in parallel arithmetic units, the method comprising:

as a result of the SIMD instructions which are converted by a Process Controlling Unit (PCU) of the signal processors, controlling parallel signal processing in the processors individually in data paths (DP) that are respectively associated with a first and a second slice;

by means of a single slice halt state that is output by a Single Slice Mode (SSM) register bank, the controlling effect of the "single slice halt" state that has been output being achieved by the bits, which are assigned to each slice, of the SSM register bank, switching the register clock supply via respective first and second gated clock cells;

as a result, stopping the functioning of the assigned input register and/or accumulator and/or pipeline control register in the meantime depending on the state of the signal processing occurring in the DP associated with the respective slice; and

enabling said functioning again only when the single slice halt state that has been output is discontinued as a result of a further SIMD instruction being converted,

wherein a register file unit (RFU) and a memory access register of the processors remain in operation irrespective of the single slice halt state that has been output and the PCU can in this case write to the SSM register bank of the PCU at any time.

2. A method for functionally controlling the program and/or data flow in digital signal processors and processors, wherein the processors have respective closed modules that are separate from one another, are intended for program and data flow control, and operate in parallel arithmetic units, the method comprising:

controlling the clock supply for a VLIW unit of the processors by means of a software-dictated output of the state from the program flow of the processors, in such a manner that, as a result, partial instruction words which are currently present in the VLIW unit are subsequently provided in the latter for multiple use at the functional units of the processors.

3. The method as claimed in claim 2, wherein the generation of further VLIWs in the VLIW unit is interrupted by a PCU of the processors being informed of a VLIW WAIT command via an advance signal line and wherein this command is applied to the PCU in the next clock cycle, the PCU then switching the clock supply for the VLIW unit by means of a VLIW WAIT signal line and a third gated clock cell of the processors.